CLAIMS:

1. A capacitor comprising:

a substrate node location;

a first container joined with the node location and having an opening defining a first interior area;

a second container joined with the node location and having an opening defining a second interior area, the areas being spaced apart from one another in a non-overlapping relationship; and

a dielectric layer and a conductive capacitor electrode layer disposed operably proximate the first and second containers.

2. The capacitor of claim 1, wherein the containers are elongate.

3. The capacitor of claim 1, wherein the containers are elongate and extend along generally parallel central axes.

4. The capacitor of claim 1, wherein the openings are generally circular in shape.

5. The capacitor of claim 1, wherein the containers are generally tubular in construction.

6. The capacitor of claim 1, wherein the capacitor comprises only two conductive capacitor electrodes separated by a dielectric region.

7. A capacitor comprising:

a substrate node location;

a first elongate container joined with the node location and extending away therefrom along a first central axis;

a second elongate container joined with the node location and extending away therefrom along a second central axis which is different and spaced apart from the first central axis; and

a dielectric layer and a conductive capacitor electrode layer disposed operably proximate the first and second containers.

8. The capacitor of claim 7, wherein the first and second central axes are generally parallel.

9. The capacitor of claim 7, wherein the containers are generally cylindrical in shape.

10. The capacitor of claim 7, wherein one of the containers is generally cylindrical in shape.

11. The capacitor of claim 7, wherein one of the containers is generally cylindrical in shape, and portions of the first and second axes are generally parallel.

12. The capacitor of claim 7, wherein each container comprises an opening away from the node location which is generally circular in shape.

13. The capacitor of claim 7, wherein the capacitor comprises only two conductive capacitor electrodes separated by a dielectric region.

14. A capacitor comprising a pair of capacitor electrodes separated by a capacitor dielectric layer, the electrodes collectively comprising first and second non-laterally-overlapping containers.

15. DRAM circuitry comprising:

a substrate node location;

a conductive layer of material disposed over and in electrical communication with the substrate node location, the layer of material having an outer surface with a first region and a second region spaced apart from the first region;

a first container formed over and in electrical communication with the first region;

a second container formed over and in electrical communication with the second region; and

a dielectric layer and a conductive capacitor electrode layer disposed operably proximate the first and second containers.

16. The DRAM circuitry of claim 15, wherein the first and second containers are generally elongate.

17. The DRAM circuitry of claim 15, wherein the first and second containers are generally elongate and extend along respective central axes, and wherein each container comprises a container portion having a generally circular transverse cross section.

18. The DRAM circuitry of claim 15, wherein the first and second containers are generally elongate and extend along respective central axes which are generally parallel with one another.

19. The DRAM circuitry of claim 15, wherein the first and second containers define container volumes which are substantially the same in magnitude.

20. The DRAM circuitry of claim 15, wherein the first and second containers are generally elongate and extend along respective central axes which are generally parallel with one another, and wherein each container comprises a container portion having a generally circular transverse cross section.

21. The DRAM circuitry of claim 15, wherein the first and second containers are generally elongate and extend along respective central axes which are generally parallel with one another, and wherein each container comprises a container portion having a generally circular transverse cross section, and wherein the first and second containers define container volumes which are substantially the same in magnitude.

22. The DRAM circuitry of claim 15, wherein the first container, the second container, the dielectric layer and the capacitor electrode layer comprise only two conductive capacitor electrodes separated by a dielectric region.

23. DRAM circuitry comprising:

a substrate having first and second spaced apart node locations;

a first storage capacitor in electrical communication with the first node location and comprising first and second containers;

a second storage capacitor in electrical communication with the second node location and comprising third and fourth containers, wherein the first, second, third, and fourth containers define container volumes which are discrete and separated from one another; and

a dielectric layer and conductive capacitor electrode layer disposed operably proximate the first and second containers.

24. The DRAM circuitry of claim 23, wherein the containers are generally elongate.

25. The DRAM circuitry of claim 23, wherein the containers are generally elongate and extend along respective central axes at least two of which being generally parallel.

26. The DRAM circuitry of claim 23, wherein the containers are generally elongate and extend along respective central axes which are generally parallel with one another.

27. The DRAM circuitry of claim 23, wherein the containers are generally elongate and extend along respective central axes, and wherein each container comprises a respective portion which has a generally circular transverse cross-section.

28. The DRAM circuitry of claim 23, wherein the containers are generally elongate and cylindrical in shape, and extend along respective central axes.

29. The DRAM circuitry of claim 23, wherein the container volumes are substantially the same in magnitude.

30. The DRAM circuitry of claim 23, wherein the containers are generally elongate and extend along respective central axes which are generally parallel with one another, and wherein each container comprises a respective portion which has a generally circular transverse cross-section, and further wherein the container volumes are substantially the same in magnitude.

31. The DRAM circuitry of claim 23, wherein the first, second, third and fourth containers, the dielectric layer and the conductive capacitor electrode layer comprise different respective capacitors having only two conductive capacitor electrodes separated by a dielectric region.

32. A method of forming a capacitor comprising:

forming a first container joined with a substrate node location, the first container having an opening defining a first interior area;

forming a second container joined with the node location, the second container having an opening defining a second interior area, the areas being spaced apart from one another in a non-overlapping relationship; and

forming a dielectric layer and a conductive capacitor electrode layer disposed operably proximate the first and second containers.

33. The method of claim 32, wherein the forming of the first and second containers comprises forming generally elongate first and second containers.

34. The method of claim 32, wherein the forming of the first and second containers comprises forming generally elongate first and second containers which extend along individual central axes which are generally parallel with one another.

35. The method of claim 32, wherein the forming of the first and second containers comprises forming the openings to be generally circular.

36. The method of claim 32, wherein the forming of the first and second containers comprises forming generally elongate first and second containers having openings which are generally circular.

37. The method of claim 32 further comprising forming said capacitor to comprise only two conductive capacitor electrodes separated by a dielectric region.

38. A method of forming a capacitor comprising:

forming a first elongate container joined with a substrate node location and extending away therefrom along a first central axis;

forming a second elongate container joined with the node location and extending away therefrom along a second central axis which is different and spaced apart from the first central axis; and

forming a dielectric layer and a conductive capacitor electrode layer disposed operably proximate the first and second containers.

39. The method of claim 38, wherein the forming of the first and second elongate containers comprises forming the containers to have central axes which are generally parallel with one another.

40. The method of claim 38, wherein the forming of the first and second elongate containers comprises forming the containers to be generally cylindrical in shape.

41. The method of claim 38, wherein the forming of the first and second elongate containers comprises forming the containers to be generally cylindrical in shape and have central axes which are generally parallel with one another.

42. The method of claim 38 further comprising forming said capacitor to comprise only two conductive capacitor electrodes separated by a dielectric region.

43. A method of forming DRAM circuitry comprising:

forming a conductive layer of material disposed over and in electrical communication with a substrate node location, the layer of material having an outer surface with a first region and a second region spaced apart from the first region;

forming a first container over and in electrical communication with the first region;

forming a second container over and in electrical communication with the second region; and

forming a dielectric layer and a conductive capacitor electrode layer disposed operably proximate the first and second containers.

44. The method of claim 43, wherein the forming of the first and second containers comprises forming the containers to be generally elongate.

45. The method of claim 43, wherein the forming of the first and second containers comprises forming the containers to be generally elongate and extend along respective central axes which are generally parallel with one another.

46. The method of claim 43, wherein the forming of the first and second containers comprises forming the containers to have volumes which are substantially the same in magnitude.

47. The method of claim 43, wherein the forming of the first and second containers comprises forming the containers to be generally elongate and have volumes which are substantially the same in magnitude.

48. The method of claim 43, wherein the forming of the first container, the second container, the dielectric layer, and the conductive capacitor electrode comprises forming a capacitor comprising only two conductive capacitor electrodes separated by a dielectric region.

49. A method of forming DRAM circuitry comprising:

providing a substrate having first and second spaced apart node locations;

forming a first storage capacitor in electrical communication with the first node location and comprising first and second containers;

forming a second storage capacitor in electrical communication with the second node location and comprising third and fourth containers, wherein the first, second, third, and fourth containers define container volumes which are discrete and separated from one another; and

forming a dielectric layer and conductive capacitor electrode layer disposed operably proximate the first and second containers.

50. The method of claim 49, wherein the forming of the first and second storage capacitors comprises forming individual containers to be generally elongate.

51. The method of claim 49, wherein the forming of the first and second storage capacitors comprises forming individual containers to be generally elongate and extend along respective central axes at least two of which being parallel.

52. The method of claim 49, wherein the forming of the first and second storage capacitors comprises forming individual containers to be generally elongate and extend along respective central axes which are parallel with one another.

53. The method of claim 49, wherein the forming of the first and second storage capacitors comprises forming individual containers to be generally elongate and cylindrical in shape and extend along respective central axes which are parallel with one another.

54. The method of claim 49, wherein the forming of the first storage capacitor, the second storage capacitor, the dielectric layer and the conductive capacitor electrode layer comprises forming different respective capacitors comprising only two conductive capacitor electrodes separated by a dielectric region.